Accordingly, the Applicant requests withdrawal of the objection to the abstract of the specification.

**The Rejection of Claim 4 Under SS 112**

The Office Action rejected dependent claim **4** on grounds of "being of improper dependent form for failing to further limit the subject matter of a previous claim." In particular, the Office Action noted that "the language 'the machine of claim 3 in which said first digital clock has a frequency that can vary, whereby the machine of claim 1'" needed clarification.

The Applicant has attempted to place claim **4** in proper dependent form by stating more clearly that "said first digital clock is a variable-frequency digital clock". The reference to "the machine of claim **1**" was removed, and the "whereby" clause was changed to more clearly express the value of having multiple digital clock frequencies.

The Applicant believes that "variable-frequency digital clock" is a considerably narrower element descriptor than "digital clock" alone, particularly in the context of integrated circuits. Many digital clocks are designed to operate at a single frequency, for instance the digital clocks that mark the passage of time in digital wristwatches, table clocks, and wall clocks. A single frequency design can be cost effective, as the oscillator driving the digital clock signal, for instance a resonant quartz crystal or a Wien bridge oscillator, can have a small number of components. On the other hand, a variable-frequency design may require more parts, such as switched multiple resonant crystals, or switched multiple RC sections in Wien bridge oscillators.

In the context of the Application, a "variable-frequency digital clock" allows for embodiments of the invention that are efficient in terms of power. Particularly, the dynamic power consumption of CMOS integrated circuits depends on the clock frequency, with a higher frequency resulting in higher consumption and a lower frequency resulting in lower consumption. A digital-to-analog converter according to the Application might be used in different applications, for instance in D/A conversion at one rate and precision for a mobile phone video screen and at another rate and precision for a mobile phone speaker. A single frequency digital clock would result in a high dynamic

power consumption for both applications. On the other hand, a variable-frequency digital clock could operate in a highest-power mode only when necessary and in lower-power modes otherwise.

**Comments on Prior Art Made of Record and Not Relied Upon**

The Office Action included a list of 8 U.S. Patents not listed in the Applicant's IDS filing that were deemed relevant to the Applicant's pending application. The Applicant includes a summary of the prior art of each reference and some comments on differences between the prior art and the present invention. The comments are in reverse chronological order by patent number.

**Comments on U.S. Patent 6,542,105 Issued to Sakuragi**

U.S. Patent 6,542,105 entitled "A/D Converter" and issued to T. Sakuragi on April 1, 2003 describes an analog-to-digital converter in which a count from a counter is passed to a digital-to-analog converter. The D/A converter output is passed as one input to a comparator, while the other input is an analog signal to be converted to a digital number value. The count is incremented until such time as the comparator output indicates that the D/A converter output has passed the level of the unknown analog signal. Then, the counter is stopped. Figure 14 of U.S. Patent 6,542,105 shows an alternative embodiment in which, rather than stopping one counter, a comparator output change triggers recording of a count in a register. In Figure 14, the counter and the digital-to-analog converter are shared among multiple rows or columns of an array of sensor cells.

In contrast, the present invention is a D/A converter, not an A/D converter. A digital count is digitally compared to one or more digital number values to be converted to analog signal values. Analog signal values are sampled and held on the basis of a digital comparison. A variety of analog reference signals are proposed, along with shared parallel D/A converters for systems where multiple D/A conversions are needed, such as image displays and other devices.

**Comments on U.S. Patent 6,392,577 Issued to Swanson et al.**

U.S. Patent 6,392,577 entitled "System and Method for Regulating an Alternator" and issued to D.F. Swanson, M. Merlo, and F. Cocetta on May 21, 2002 describes a device in which a relatively low-frequency (20 kHz) clock drives a relatively low-precision (8-bit) downward counter. The downward counter's output is supplied to a D/A converter, resulting in a relatively low-frequency (78.125 Hz) sawtooth wave. The sawtooth wave is compared to an amplified error voltage. The resulting comparator output is a pulse-width modulated (PWM) control signal whose duty cycle is determined by the relative proportion of time that the sawtooth waveform is greater than the amplified error signal. The PWM comparator output or a digital version of the same (per figures 6A and 6B respectively) is passed to a Field Driver Circuit which ultimately controls an alternator.

The present invention is a D/A converter, and can use sawtooth analog reference waves in some embodiments, but is not intended primarily to generate a PWM control signal for an electromechanical engine part.

**Comments on U.S. Patent 5,909,186 Issued to Göhringer**

U.S. Patent 5,909,186 entitled "Methods and Apparatus for Testing Analog-to-Digital and Digital-to-Analog Device Using Digital Tester" and issued to R. Göhringer on June 1, 1999 describes an approach to testing mixed-signal circuits - in other words, systems or semiconductor chips with both analog and digital functions - using a digital testing device rather than a specialized mixed-signal testing device. In embodiments of the invention for testing A/D converter circuits, the digital tester provides digital conversion control signals and a reference A/D converter output from a D/A converter known to be good. By comparing the digital input to the known-good D/A converter with the output of an A/D converter being tested it is possible to assess whether or not the latter is functioning properly. Similarly, the digital tester can provide digital conversion control signals to a D/A converter to be tested. The D/A converter output is passed to the input of an A/D converter known to be good. The digital converter can compare the known-good A/D converter output to the digital inputs provided to the D/A converter under test.

Whereas U.S. Patent 5,909,186 treats both A/D and D/A converters at the converter block level, the present invention is a D/A converter with detailed parts. The counting and comparison in U.S. Patent 5,909,186 is aimed at testing the performance of mixed-signal devices by applying a finite set of digital test signals and examining the results of a D/A-then-A/D conversion, one half of which is known to be good. Counting and comparison in the present invention is aimed at D/A conversion, particularly in massively parallel conversion applications.

**Comments on U.S. Patent 5,572,211 Issued to Erhart et al.**

U.S. Patent 5,572,211 entitled "Integrated Circuit for Driving Liquid Crystal Display Using Multi-Level D/A Converter" and issued to R.A. Erhart and T. W. Ciccone on November 5, 1996 describes D/A conversion circuitry for the column driver of an LCD display.

The invention has a time-varying clock signal which causes a digital count provided by a digital counter to change. The time-varying clock signal also causes selection of various sets of possible analog outputs. Portions - for instance, a certain number of most-significant bits - of digital numbers to be converted to LCD driver voltages are compared to the count. When the portions match, other portions - for instance, the remaining least significant bits - are used to select from among the set of possible analog outputs at that count value. For multiple analog values per count signal, the invention proposes resistor networks similar to those of flash A/D converters, with switching of network tap points

The present invention is a D/A converter which is useful in LCD displays but also in other devices such as acoustic speakers, or in multiple devices simultaneously. The analog reference source can provide non-discrete analog signal values during the period of a given count value, for instance, an increasing ramp or a segment of another function, which may be linear or nonlinear, such as a sinusoid. The analog reference source can be free-running after a triggering signal, rather than relying on clock-governed switches at each count increment. With a free-running non-discrete analog reference source, switching among multiple reference signals is not necessary, nor is it necessary to have a delay to allow for reference signal settling during conversion.

**Comments on U.S. Patent 5,920,273 Issued to Hirano et al.**

U.S. Patent 5,920,273 entitled "Digital-to-Analog Converter" and issued to M. Hirano on July 6, 1999 describes a D/A converter based on sigma-delta (also known as "delta-sigma") modulation. A principal goal of the invention is to preserve the effects of a dither signal which prevents converter output oscillation during periods of no converter inputs while allowing for a variable DC offset of the analog output.

Recall that a delta-sigma converter uses involves selectively integrating (or summing, and hence the "sigma" in the name) small parcels of charge (of size "delta"). A comparator output is used to determine whether or not to add a charge parcel at each clocking interval. For a delta-sigma D/A converter, the analog staircase is filtered to produce a desired analog output.

In U.S. Patent 5,920,273, a filtered analog output with an added DC offset is compared to a reference voltage during a calibration period. During calibration, an up-down counter determines the relative portion of time at which the filtered-plus-offset output is above or below a reference voltage, and consequently the actual DC offset. The resulting count is used to select a correcting DC offset to use.

As a D/A converter, the idea of the present invention is not a delta-sigma modulator. Since the summation in a delta-sigma modulator is selective, it is fundamentally unsuited for parallel implementations in which differing digital inputs result in differing analog outputs.

**Comments on U.S. Patent 5,426,413 Issued to Gulczynski**

U.S. Patent 5,426,413 entitled "High Speed Integrating Digital-to-Analog Converter" and issued to Z. Gulczynski on June 20, 1995 describes a multiple-slope integrating D/A converter. The invention includes two or more downward counters which control switches connected to current sources, integrating capacitors, or both. Based on the count values, the amount of current being integrated or the size of the capacitor being charged can be changed. Thus, a D/A converter can have a very high analog signal slew rate during an early stage of conversion, followed by a lower slew rate during a

later stage. The former allows fast conversion first, while the latter enables precision near the end of the conversion cycle, when, presumably, only a small adjustment in the reconstructed analog signal remains necessary.

**Comments on U.S. Patent 4,544,911 Issued to Altman et al.**

U.S. Patent 4,544,911 entitled "Low Cost Monotonic Digital-to-Analog Converter" and issued to T.N. Altman and N.J. Fedele on October 1, 1985 describes a D/A converter for a television tuner which is intended to have high resolution (number of bits) at low cost. The analog output to the television tuner is ultimately a filtered sum of a coarse pulse-width modulated signal and a fine pulse-width modulated signal. In the patent, the term "digital-to-duty factor" is used to describe a PWM system.

As discussed above for U.S. Patent 6,392,577, the present invention is not a D/A converter based on filtered PWM signals.

**Comments on U.S. Patent 4,381,495 Issued to Hotta et al.**

U.S. Patent 4,381,495 entitled "Digital-to-Analog Converter with Error Compensation" and issued to M. Hotta, K. Maio, N. Yokozawa, and H. Nagaishi on April 26, 1983 describes a D/A converter system with a calibration and correction stage. The calibration is performed by comparing the analog output corresponding to a given digital input to a voltage ramp. The comparison result is used to generate a digital number representative of the portion of time the voltage ramp is greater than (or alternatively, less than) the analog output. This is effectively an A/D conversion. The count is then compared to the input to determine a digital correction that is then stored in a table.

The present invention is a D/A converter intended to enable parallel conversion with a common time-varying analog reference signal, and possibly also with a common counter. The present invention does not include specific circuitry for A/D conversion of D/A converter outputs and subsequent digital look-up table correction.

## CONCLUSION

For all of the above reasons, the Applicant submits that the specification and the claims are now in proper form, and that the claims are all patentable over the prior art. Therefore, the Applicant submits that this application is now in condition for allowance, which action is respectfully solicited.

**Conditional Request for Constructive Assistance**

The Applicant has amended the specification and claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, the Applicant, an independent inventor and pro se filer, respectfully requests the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P SS 2173.02 and SS 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.



Very Respectfully,

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May 5, 2003 Charles Douglas Murphy

Charles Douglas Murphy, Applicant